CLAIMS

What is claimed is:

1. An input/output controller integrated circuit comprising:

a host interface subsystem to couple to a host to receive host commands and to transceive data blocks with the host in response to the host commands;

and

a mapping controller coupled to the host interface subsystem, the mapping controller to map logical block addresses of the host commands into physical block addresses of one or more peripherals to transceive the data blocks with the one or more peripherals.

2. The integrated input/output controller of claim 1 further comprising:

a peripheral interface subsystem to couple to the one or more peripherals to issue peripheral commands and to transceive data blocks with the one or more peripherals in response to the one or more peripheral commands.

3. An integrated input/output (I/O) controller integrated into an integrated circuit to read and write data between a host and one or more peripherals, the integrated I/O controller including circuits to perform:

receiving a high level I/O command from a host;

parsing the high level I/O command to determine whether to read or write data;

mapping the high level I/O request into one or more peripheral I/O commands, the one or more peripheral I/O commands indicating which of the one or more peripherals and which respective data locations are to be accessed; and

servicing the high level I/O request by reading or writing data between the host and the one or more peripherals using the respective data locations.

4. The integrated I/O controller of claim 3, further including circuits to perform:

prior to servicing the high level I/O request, storing data temporarily into an external cache buffer from the data flow between the host and the one or more peripherals.

5. The integrated I/O controller of claim 3, wherein,

each of the one or more peripheral I/O commands further indicates the number of blocks of data to be serviced.

6. The integrated I/O controller of claim 3, wherein,

mapping the high level I/O request into one or more peripheral I/O commands includes circuits to perform

parsing a high level command from an I/O request packet,

decoding the high level command and generating a range operation request in response thereto, and generating the one or more peripheral I/O commands in response to the range operation request.

7. The integrated I/O controller of claim 3, wherein, each of the one or more peripherals are storage disks and each of the one or more peripheral I/O commands are Small Computer System Interface (SCSI) disk I/O commands.

8. The integrated I/O controller of claim 3, wherein, the high level I/O command is a command of a Small Computer System Interface (SCSI) Command Descriptor Block (CDB) standard.

9. The integrated I/O controller of claim 3, wherein, the circuits of the integrated I/O controller are hard wired circuits.

10. The integrated I/O controller of claim 3, wherein, the circuits of the integrated I/O controller are microcoded circuits and state machines operating concurrently.

11. The integrated I/O controller of claim 3, wherein,

the circuits of the integrated I/O controller are hard wired circuits, microcoded circuits and state machines operating concurrently.

12. The integrated I/O controller of claim 3, wherein, the circuits of the integrated I/O controller are programmable micro-controllers operating concurrently.

13. An input/output controller integrated into a single integrated circuit comprising:

a host interface subsystem to couple to a host to receive host commands and to transceive data blocks with the host in response to the host commands;

a peripheral interface subsystem to couple to a peripheral to issue peripheral commands and to transceive data blocks with the peripheral in response to the peripheral commands; and

a mapping controller coupled to the host interface subsystem and the peripheral interface subsystem, the mapping controller to map to blocks of data storage of the peripheral.

14. The integrated input/output controller of claim 9 further comprising:

a micro-controller subsystem coupled to the host interface subsystem and the peripheral interface subsystem,

the micro-controller subsystem to perform initialization and to process errors and exception events.

15. The integrated input/output controller of claim 13 further comprising:

a cache manager coupled to the host interface subsystem and the peripheral interface subsystem, the cache manager to manage entries in a cache buffer to temporarily store data of the data flow between the peripheral and the host.

16. The integrated input/output controller of claim 15 further comprising:

a buffer manager coupled to the host interface subsystem, the peripheral interface subsystem, and the cache manager, the buffer manager to manage data storage in the cache buffer.

17. The integrated input/output controller of claim 13 wherein,

the host interface subsystem includes a fibre channel host port to transceive data with the host using a fibre channel protocol.

18. The integrated input/output controller of claim 13 wherein,

the host interface subsystem includes

a host exchange controller to control the physical connection and protocol of the host.

19. The integrated input/output controller of claim 13 wherein,

the host interface subsystem includes

a command decode controller to decode host commands.

20. The integrated input/output controller of claim 13 wherein,

the peripheral interface subsystem includes

a peripheral exchange controller to control the physical connection and protocol of the peripheral.

21. The integrated input/output controller of claim 13 wherein,

the peripheral interface subsystem includes a Fibrechannel disk port to transceive data with the peripheral using a Fibrechannel protocol.

22. A method of processing host write commands between a host and one or more peripherals, the method comprising:

receiving a high level write command from a host, the high level write command requesting to write data from the host transparently to one or more peripherals;

mapping the high level write command into one or more low level peripheral write commands, the one or more low level peripheral write commands indicating data storage locations in the one or more peripherals into which data from the host is to be written;

servicing the high level write command by receiving data from the host for storage into the data storage locations in the one or more peripherals; and

writing the data from the host into the data storage locations in the one or more peripherals in response to the one or more low level peripheral write commands.

23. The method of claim 22 further comprising:

prior to writing the data from the host into the data storage locations, temporarily storing the data from the host into a buffer memory.

24. The method of claim 22 wherein,

the high level write command indicates the number of blocks of data to be written from the host.

25. A method of processing host read commands between a host and one or more peripherals, the method comprising:

receiving a high level read command from a host, the high level read command requesting to transparently read data from the one or more peripherals to the host;

mapping the high level read command into one or more low level peripheral read commands, the one or more low level peripheral read commands indicating data storage locations in the one or more peripherals from which data is to be accessed and read out to the host;

servicing the high level read request by reading data from the data storage locations in the one or more peripherals in response to the one or more low level peripheral read commands; and

providing the data to the host.

26. The method of claim 25 further comprising:

prior to providing the data to the host, temporarily storing the data from the one or more peripherals into a buffer memory.

27. The method of claim 25 wherein,

the high level read command indicates the number of blocks of data to be read into the host.

28. An integrated input/output controller comprising:

a semiconductor integrated circuit including,

a host interface to couple to one or more servers to transceive data between the one or more servers and the integrated input/output controller in response to host commands,

a mapping controller coupled to the host interface subsystem, the mapping controller to map to blocks of data storage of a peripheral, and

a micro-controller coupled to the host interface subsystem, the micro-controller to perform initialization and handle error and exception handling events.

29. The integrated input/output controller of claim 28 wherein,

the host interface subsystem includes a fibre channel host port to transceive data with the one or more servers using a fibre channel protocol.

30. The integrated input/output controller of claim 28 wherein,

the host interface subsystem includes a command decode controller to receive and decode host command packets.

31. The integrated input/output controller of claim 30 wherein,

the command decode controller to further validate a host command and to initiate execution of the host command by the integrated input/output controller.

32. The integrated input/output controller of claim 30 wherein,

the command decode controller to further validate a host command and to queue the host command in a queue to be executed in an order, the command queue associated with a volume accessible by one of the one or more a servers.

33. The integrated input/output controller of claim 30 wherein,

the command decode controller to further validate a host command and to determine that the host command is invalid, the host command is passed to the micro-controller subsystem to process the invalidity.

34. The integrated input/output controller of claim 30 wherein,

the host command packets are high level input/output requests.

35. The integrated input/output controller of claim 28 further comprising:

a peripheral interface to couple to one or more peripheral devices and transceive data between the one or more peripheral devices and the one or more servers coupled to the host port.

36. The integrated input/output controller of claim 28 wherein,

the integrated input/output controller is an integrated RAID controller to transceive data between one or more disks of at least one disk array and the integrated input/output controller further comprises:

a disk interface to couple to the one or more disks of the at least one disk array to transceive the data to or from the one or more servers; and

the mapping controller is a RAID mapping controller to flexibly control the mapping of blocks of data storage on the one or more disks of the at least one disk array.

37. The integrated input/output controller of claim 36 wherein,

the one or more disks of the at least one array of disks are magnetic storage media, optical storage media or semiconductor storage media.

38. The integrated input/output controller of claim 36 wherein,

the disk interface subsystem includes one or more fibre channel disk ports to transceive data with the one or more disks of the at least one disk array using a fibre channel protocol.

39. The integrated input/output controller of claim 28 wherein,

the mapping controller provides RAID mapping automation.

40. The integrated input/output controller of claim 28 wherein,

the mapping controller is programmable hardware to flexibly control the mapping of blocks of data storage on the one or more disks of the at least one disk array.

41. The integrated input/output controller of claim 28 wherein,

the mapping controller to receive a requested command input packet to generate expanded command output packets in response thereto, the requested command input packet functions as a logical address and the expanded command output packets function as physical addresses.

42. The integrated input/output controller of claim 28 further comprising:

a buffer manager and a cache manager, the buffer manager and the cache manager to couple to a cache buffer and a cache table buffer respectively to flexibly control the reading and writing of data to and from the mapped data storage on the one or more disks of the at least one disk array.

43. A storage area network for central data storage and management, the storage area network comprising:

at least one server to couple to a network;

at least one disk array having a plurality of disks; and

at least one fibre channel controller to couple to at least one server and at least one disk array, the at least one fibre channel controller to read and write data between the at least one server and the at least one disk array, the at least one fiber channel controller having

a cache memory,

a microprocessor to initialize the fiber channel controller upon power up and reset,

a programmable random access memory (PRAM) to store initialization instructions in firmware, and

a hardware redundant array of independent disks (RAID) controller to control the reading and writing of data between the at least one server and the at least one disk array.

44. The storage area network of claim 43 for central data storage and management, wherein the hardware RAID controller includes,

a host interface to couple to the at least one server to receive data from the at least one server for storage into the one or more disks of the at least one disk array and to transmit data to the at least one server for data accessed from the one or more disks of the at least one disk array;

a disk interface to couple to the one or more disks of the at least one disk array to transmit data to the one or more disks of the at least one disk array

for storage and to receive data from the one or more disks of the at least one disk array when accessed,

a RAID mapping controller to flexibly control the mapping of blocks of storage on the one or more disks of the at least one disk array, and

a micro-controller coupled to the host interface subsystem, the disk interface subsystem, and the RAID mapping subsystem, the micro-controller to handle non-data flow commands, error and exception handling events as well as system initialization.

44. The storage area network of claim 43 for central data storage and management, wherein,

the cache memory to provide a cache data buffer and a cache table buffer for the integrated RAID controller integrated circuit.

46. The storage area network of claim 43 for central data storage and management, wherein,

the plurality of disks of the at least one array of disks are magnetic storage media, optical storage media or semiconductor storage media.

47. An integrated input/output (I/O) controller comprising:

a semiconductor integrated circuit including,

a host command manager to manage high level host I/O requests from a plurality of hosts;

a mapping engine to map high level host I/O requests into low level I/O commands; and

a low level command manager to manage data read and data write accesses into and out of a peripheral device in response to the low level I/O commands.

48. The integrated input/output (I/O) controller of claim 47 further comprising:

a buffer manager to arbitrate access by the one or more servers and to control data reads and data writes into and out of a buffer memory.

49. The integrated input/output (I/O) controller of claim 47 further comprising:

a micro-controller to handle non-data flow commands, system initialization and error handling exception conditions.

50. The integrated input/output (I/O) controller of claim 47 wherein

the integrated I/O controller is a RAID controller and the peripheral device is a plurality of disks responsive to disk I/O commands.

51. A method of transceiving data to a plurality of disks in an integrated circuit, the method comprising:

receiving an I/O request from at least one server, the I/O request indicating a volume to access;

mapping the I/O request into a disk I/O command, the disk I/O command indicating one or more disks of the plurality of disks to process the disk I/O command; and

managing a data read or a data write access to the plurality of disks in response to the disk I/O command.

52. The method of claim 51 for transceiving data to a plurality of disks in an integrated circuit further comprising:

arbitrating a data read or a data write access to a buffer memory to temporarily store the data prior to the data read or data write access to the plurality of disks.